Beijing-Dublin International College

SEMESTER 2 FINAL EXAMINATION - 2020/2021

BDIC3001J Computer Architectures

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Time Allowed: 95 minutes

Instructions for Candidates

BJUT Student ID: _____UCD Student ID: _____

I have read and clearly understand the Examination Rules of both Beijing University of Technology and University College Dublin. I am aware of the Punishment for Violating the Rules of Beijing University of Technology and/or University College Dublin. I hereby promise to abide by the relevant rules and regulations by not giving or receiving any help during the exam. If caught violating the rules, I accept the punishment thereof.

Honesty Pledge：_____ (Signature)

Instructions for Invigilators

All electronic devices, notebooks, books, work papers are strictly prohibited.

Obtained score

Part 1: Single-Choice Questions (15 marks)

1. Which one of the following is not transparent to computer architecture? ( )
   - A. Buffering technology
   - B. The width of data bus
   - C. The speed of main memory
   - D. Operating mode

2. The meaning of data representation is ( ).
   - A. Data type
   - B. Data types which can be directly identified by hardware
   - C. The representation of floating point numbers
   - D. The code system which can be used to represent data

3. Custom data representation of multidimensional array usually adopts ( ).
   - A. Floating-point data representation
   - B. Data representation with identifier
   - C. Data descriptor
   - D. Fixed-point data representation

4. The code which has the shortest average code length is ( ).
   - A. Huffman encoding
   - B. Fixed-length code
   - C. Need to determine after calculating according to the code frequency
   - D. Extension code

5. Instruction system encoding method does not include which of the following. ( )
   - A. Integral method
   - B. Address method
   - C. Hybrid method
   - D. Orthogonal method

6. Which of the following does not belong to the memory protection method? ( )

A. Directory protection B. Boundary protection

C. Key protection D. Ring protection

7. The Cyclic Representation of the interconnect function $PM2_{-2}$ is ( ).

A. （0 2）(4 6)（1 3）(5 7）

B. （0 1 2 3 4 5 6 7）

C. （6 4 2 0）（7 5 3 1）

D. （0 4）(1 5) (2 6) (3 7）

8. The program locate mode does not include which of the following. ( )

A. Static locate mode

B. Dynamic locate mode

C. Indirect locate mode

D. Direct locate mode

9. In the multilevel hierarchy of computer systems, from the lower level to the upper level, the correct relative order at all levels should be ( ).

A. Algorithm -- Operating system -- Programming language

B. Instruction set architecture -- Register transfer level-- Operating system

C. Register transfer level --Microarchitecture-- Programming language

D. Application--Register transfer level--Operating system

10. The processing method of control hazard in the pipelining processor does not include ( ).

A. Forwarding

B. Static branch prediction

C. Form condition code in advance

D. Dynamic branch prediction

11. Which of the following processors implements parallel processing by using the concept of resource replication? ( )

A. Pipeline processor B. Superscalar processor

C. Parallel (array) processor D. Associative processor

12. The number of the 16 processors is 0~15. They are connected by the interconnection network, and the interconnection function is Shuffle^{-1} (PM2$_{+3}$).
The processor number to which the 11th processor will be connected is ( ).
A. 5 B. 9 C. 13 D. 3

13. RISC adopts overlapping register window technology, thus greatly reduces ( ).
A. Memory access time
B. The execution time of most instructions
C. The number of instruction of target program
D. The number of accessing memory due to program calls

14. The static pipelining refers to ( ).
A. The multiple function pipelining can only do one function at the same time
B. The pipelining with only one function
C. The pipelining can perform multiple functions at the same time
D. The pipelining in which the function can't change

15. Which of the following is related to the maximum throughput rate of pipelining? ( ).
A. The last sub-process time
B. The fastest sub-process time
C. Each sub-process time
D. The slowest sub-process time

Obtained score

Part 2: Sentence Completion (10 marks)

1. In cache and memory systems, each time cache hits, the CPU only writes to cache, this method is called _____ .
2. Vector pipelining processor has two kinds of structure, are respectively _____ and _____ .
3. In order to achieve software portability, we should strive to the software _____ compatibility, and make sure the software _____ compatibility.
4. Flynn classification is based on the multiplicity of _____and _____.
5. The major methods for increasing memory bandwidth usually include _____, _____ and _____ .

Obtained score

Part 3: Short-Answer Questions (5 marks)

1. **Please describe briefly the three main techniques of RISC. (3 marks)**

2. **Which two methods are used for interrupt handling in the instruction pipelining? (2 marks)**

Obtained score

Part 4: Calculation Questions (70 marks)

1. **A computer with a 800 MHZ processor executes the target code including 70000 instructions, the program is mainly composed of four kinds of instruction. According to the program tracking experiment result, the proportion of instruction and the CPI of each kind instruction required are as follows. (6 marks)**

Instruction Type	Proportion	CPI
ALU	34%	4
Load	19%	5
Store	24%	4
J	23%	2

Please try to get the value of average CPI, MIPS and the total execution time.

2. **Assume that the mapping mode between cache and main memory is set associative mapping. Main memory consists of 16 blocks of B0 ~ B15, cache has 2 groups, each group contains 4 pieces, each block size is 64 bytes, FIFO replacement algorithm is used. When a program is executed, the block address stream is as follows:**

2,7,8,11,14,12,14,2,9,6,7,1,15,10,4,13,9,3

(1) Please write out the format of the main memory address, and mark the length of each field.
(2) Please write out the cache address format, and mark the length of each field.
(3) Please write out the format of the directory table required for address mapping transformation, mark the length of each field, and indicate the capacity of the directory table.
(4) Please calculate the cache block hit rate. (10 marks)

3. MIPS binary codes, including 8 instructions, are shown in the following table. Assume that registers $6 holds the base address of the integer array A.

(1) Please disassemble this code.

(2) Please show the contents of the register $10 and A[1] when the program is finished.

(3) When this code runs as the manner of pipelining, which instructions will cause control hazards? Please write down the numbers of these instructions.

(11 marks)

Note:

SUBU:	**opcode:**	**000000**
	funct:	**100011**
ADDI:	**opcode:**	**001000**
ORI:	**opcode:**	**001101**
SW:	**opcode:**	**101011**
BEQ:	**opcode:**	**000100**
J:	**opcode:**	**000010**

No.	Address	Code
1	0x00003000	0x34080064
2	0x00003004	0x34090005
3	0x00003008	0x01094023
4	0x0000300c	0x214a0001
5	0x00003010	0xacc80000
6	0x00003014	0x20c60004
7	0x00003018	0x11000001
8	0x0000301c	0x08000c02

4. There are ten instructions in a machine and the use probability is respectively:

0.26, 0.2, 0.15, 0.09, 0.08, 0.06, 0.06, 0.05, 0.03, 0.02.

(1) Calculate the average coding length of the fixed-length code.

(2) Form a Huffman tree.

(3) Get the Huffman coding and calculate the average coding length.

(4) If the extension coding can only have two kinds of length, please design the Huffman extension coding scheme to get the shortest average coding length.

(10 marks)

5. Assume that a dual-function static pipelining can execute addition and multiplication and include 5 stages, named as S1, S2, S3, S4, S5. The connection of addition is S1→S3→S5, the connection of multiplication is S1→S2→S4→S5. The processing time for S4 is 2△t and the processing time for other each stage is △t. Now calculate the following formula

$$\sum_{i=1}^{3}[(\boldsymbol{a_i} * \boldsymbol{b_i}) + \boldsymbol{c_i}]$$

Please draw the spatial-temporal chart which can get the optimal throughput rate and write out the total calculation time and get T_P, η and Sp. (10 marks)

6. **The following is the reservation table of a four-stages non-linear pipelining. Please write out the forbidden list (F) and the collision vector (C). Please draw the state transition diagram and get the minimum average latency, the maximum throughput rate and the best scheduling policy. If you use this scheduling policy to input 6 tasks, please write out the actual throughput rate. (10 marks)**

t / s	t1	t2	t3	t4	t5	t6	t7
s1	×						×
s2		×					
s3			×		×		
s4				×		×	

7. **Assume that in the CRAY-1 vector machine, V is the vector register and the vector length are 64. S is the scalar register. The floating-point addition needs 6 Δt , the floating-point multiplication needs 7 Δt , memory access needs 6 Δt . The set-up time of vector register and memory is both 1 Δt.**

   What is the best execution process of the following instruction set, and according to the best solution to calculate the total processing time. (5 marks)

$$V1 \leftarrow V2+V3$$
$$V6 \leftarrow V1*V5$$
$$V0 \leftarrow V6+V4$$
$$S2 \leftarrow S3+S4$$
$$V5 \leftarrow M$$
$$V1 \leftarrow V0*V5$$

8. **Assume that N = 8, please draw the corresponding Omega network. In order to realize the 4th processor are connected with processor 0 to 5, at the same time, the 5th processor are connected with processor 6 to 7, how to set up the cross switch?**

   (8 marks)