



Beijing-Dublin International College



SEMESTER 2 FINAL EXAMINATION - 2020/2021

EEEN3013J Advanced Electronics

MODULE COORDINATOR: XIULONG BAO

Time Allowed: 120 minutes

Instructions for Candidates

BJUT Student ID: _____ UCD Student ID: _____

I have read and clearly understand the Examination Rules of both Beijing University of Technology and University College Dublin. I am aware of the Punishment for Violating the Rules of Beijing University of Technology and/or University College Dublin. I hereby promise to abide by the relevant rules and regulations by not giving or receiving any help during the exam. If caught violating the rules, I accept the punishment thereof.

Honesty Pledge: _____ (Signature)

Problem1 (30%)

1. An op-amp has the maximum output voltage of 0.5V and maximum signal frequency is 1.0×10^6 rad/s. Its specified slew rate is _____ V/ μ sec.
2. An op-amp inverting amplifier uses a feedback resistor of 500 k Ω and input resistor of 5 k Ω . If the op-amps input offset voltage is 4.0 mV and input offset current is 150nA, the amplifier output offset voltage is _____.
3. For the circuit shown in Fig.1b, the input is triangular waveform (Fig.1a), sketch the output waveform on the given axis.

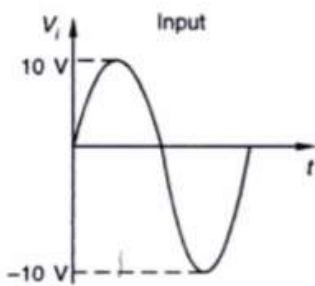


Fig.1a

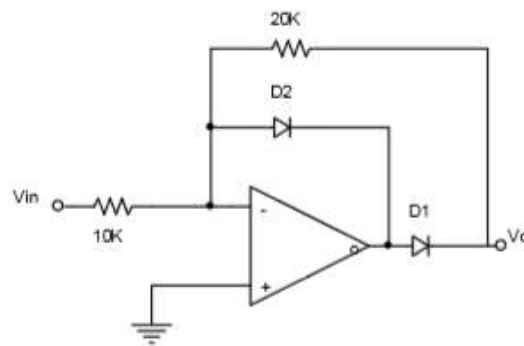


Fig.1b

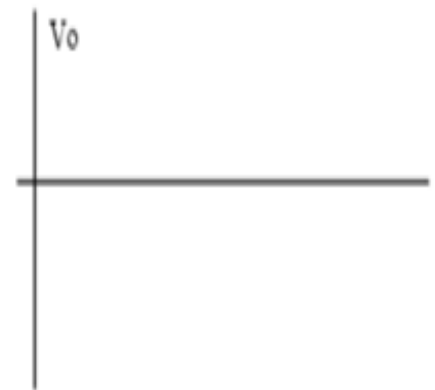


Fig.1c

4. The ac equivalent circuit of a crystal in the Fig.2 has the values: $L = 4$ H, $C_s = 0.04$ pF, $R = 1$ k Ω , and $C_m = 5$ pF. Its parallel resonant frequency is _____ Hz.

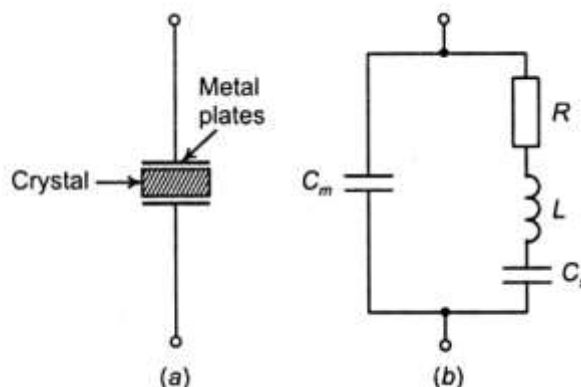


Fig.2

5. In the voltage regulator circuit shown in the Fig.3, the op-amp is ideal. The BJT has $V_{BE} = 0.7\text{V}$ and $\beta = 100$, and the Zener voltage is 4.7V . For a regulated output of 9V , the value of R (in Ω) is _____.

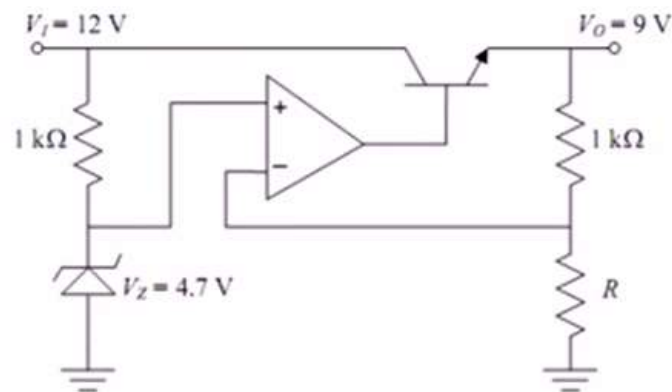


Fig.3

6. For a class B amplifier providing a 20-V peak signal to a 16Ω load (speak) and a power supply of $V_{CC} = 30\text{V}$, the input power is _____, the output power is _____, and the circuit efficiency is _____

Problem2 (20%)

- (i) Find the oscillation frequency and condition for oscillation for the following modified phase shift oscillator circuit.

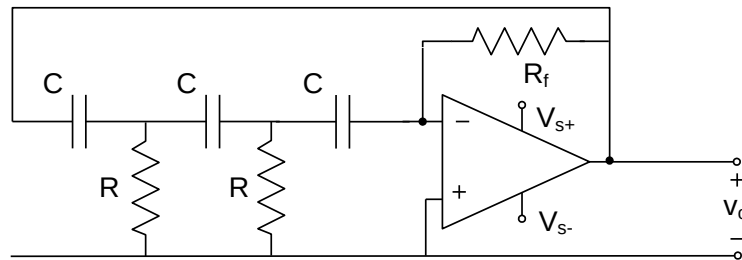
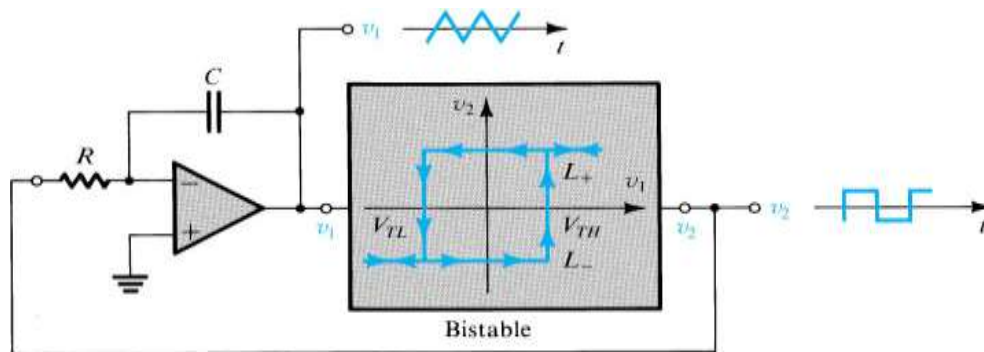
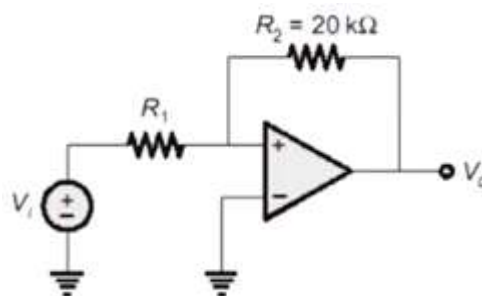


Fig.4 The modified phase shift oscillator circuit

- (ii). In the bistable circuit shown in Fig.5, the ideal OPAMP has saturation levels of $\pm 5V$. The value of R_1 (in $k\Omega$) that gives a hysteresis width of 500mV is _____.



(a)



(b)

Fig.5

Problem3 (15%)

Calculate voltage V_1 , V_2 , V_3 , and specify the operation region of all the transistors. You must clearly show the procedure/ proof of your answer.

$K'_n = 100 \mu\text{A}/\text{V}^2$, $K'_p = 50 \mu\text{A}/\text{V}^2$, $V_{tn} = 0.5 \text{ V}$, $V_{tp} = -0.5 \text{ V}$, $\lambda_{n/p} = 0$.

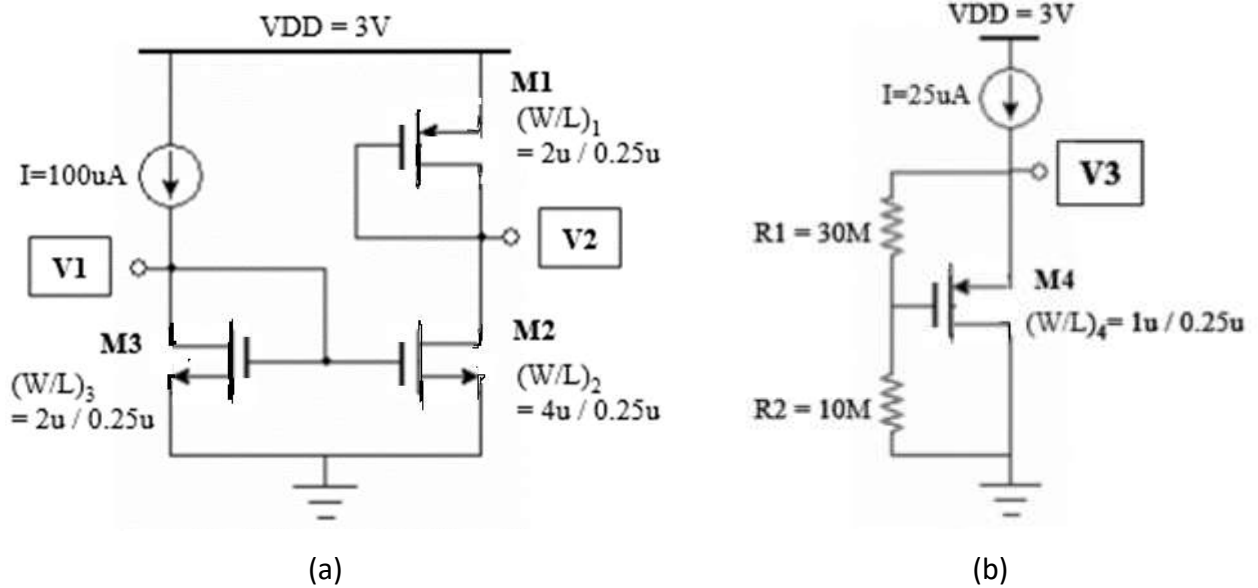


Fig. 6

Problem4 (20%)

Consider an 8-bit DAC as shown in Fig.7 with $V_R = 5\text{ V}$.

- (i) What is the smallest value of R which will limit the current drawn from the supply (V_R) to 10mA?
- (ii) If $R_f = R$, what is the resolution (i.e., ΔV_A corresponding to the input LSB changing from 0 to 1 with other input bits constant)?
- (iii) What is the maximum output voltage (in magnitude)?
- (iv) Find the output voltage corresponding to the input 1010 1101.

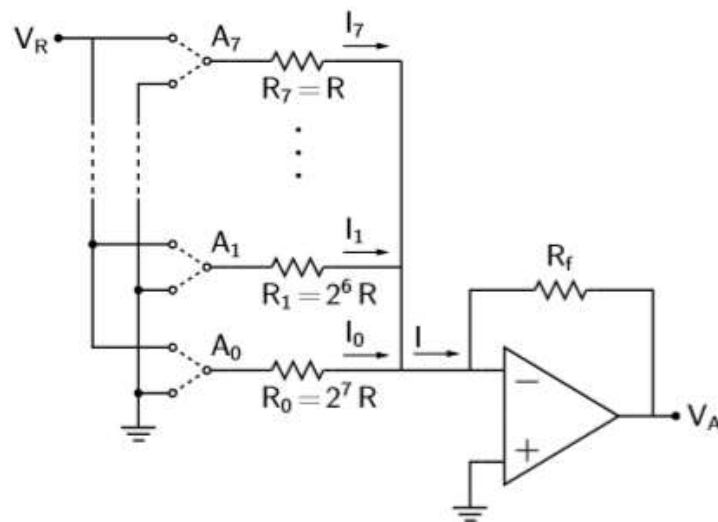


Fig.7

Problem5 (15 %)

1. Assume the op amp exhibits an open-loop gain of A_1 , but is otherwise ideal. Also $\lambda = 0$. Calculate the loop gain of the circuits illustrated in Fig.8.

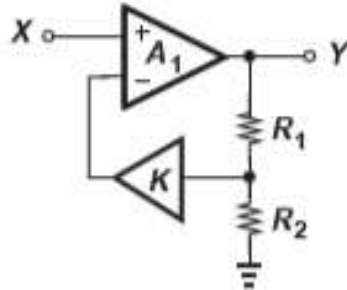


Fig. 8

2. For the bipolar circuits depicted in Fig.9, identify all of the transistor capacitances and determine which ones are in parallel and which ones are grounded on both ends

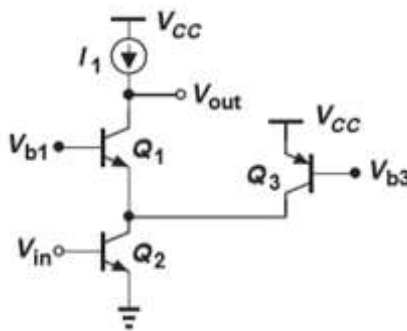


Fig.9

3. A buck converter shown in Fig.10 has a DC input voltage V_i of 10 V. The required average output voltage V_o is 5 V with a peak-to-peak output ripple of 20 mV. The switching frequency is 25 kHz. The peak-to-peak ripple current of the inductor is limited to 0.8 A.

- Calculate the duty cycle.
- Calculate the minimum value of the filter inductance L .

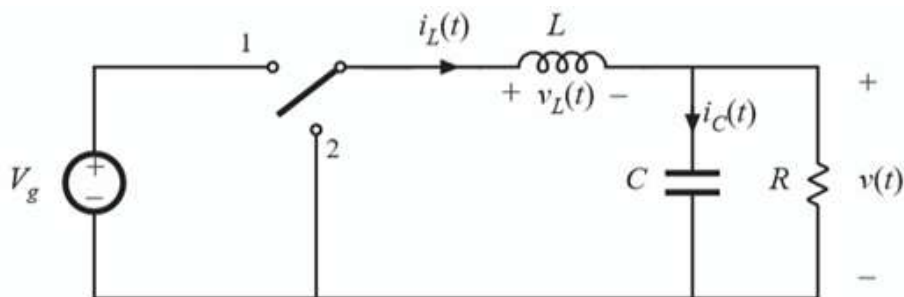


Fig.10